LISTING OF CLAIMS

1-62: (Cancelled)

63. (Previously Presented) A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

64. (Previously Presented) A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into more than two states in order to store more than one bit of data per cell, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.

65. (Previously Presented) A flash memory card having a plurality of flash memory partitions each of which is divided into a plurality of physical blocks, each of the physical blocks having a plurality of flash memory cells, each flash memory cell being individually programmable into two states in order to store one bit of data per cell, comprising:

a connector for connecting said flash memory card to an external device;

a data control logic circuit for controlling a transfer of data between the outside of said flash memory card and the plurality of flash memory partitions through said connector and respectively transmitting block erase commands to the flash memory partitions including the physical blocks to be erased when the block erase commands associated with a plurality of blocks are inputted via said connector; and

an address control logic circuit for managing addresses for the plurality of blocks inputted via said connector so as to disperse into the plurality of flash memory partitions by assigning the addresses to their corresponding addresses for the physical blocks of the plurality of flash memory partitions and for respectively transmitting chip enable signals to at least two of the plurality of flash memory partitions including the physical blocks to be erased in such a manner that when the block erase commands are inputted via said connector, a period in which said at least two flash memory partitions are simultaneously busy, exists.